



---

**SERCON816**  
**SERCOS interface Controller**

Reference Manual  
Version 7.4, 04/2003

---

**Project:** SERCON816  
**Document Type** Reference Manual  
**File:** SERCON816man-v7\_4.doc

<b>Version</b>	<b>Date</b>	<b>Remarks</b>
08/99	August 24, 1999	Preliminary edition
<b>Version</b>	October 12, 1999	Add Nandtree Description
01/2000	November 5, 1999	Final modifications (TWG)
04/2000	April 2000	Editorial correction, setup time, hold time
10/2000	October 2000	New Fig. 17: Data and clock regeneration
07/2001	July 2001	Table of MCLK, current consumption
	October 2001	Clear Interrupt Timing (WRN -> INT 0/1)
02/2002	February 4, 2002	correction for RegMode=1
09/2002	September 24, 2002	TQFP Packaging mechanical information removed
		Correction Fig. 48 (Missing sync telegrams)
01/2003	January 2003	Fig. 19 Transmitter circuit
		TxD6-1, peak / static output current
7.4	April 2003	Chapter G: Troubleshooting added
		Correction of BUSYN Timing Description (page 23)

The Interests Group SERCOS interface e. V. is not liable for any errors in this documentation. Liability for direct and indirect damages arising in connection with the supply of this documentation is excluded in so far as it can be attached legally.

This documentation contains copyright-protected information.

All rights, especially the right of duplication, distribution and translation, are reserved. No portion of the documentation may be reproduced, copied or distributed in any form (photocopy, microfilm or other process) without advance written permission of the Interests Group SERCOS interface e. V.

Published by

Interests Group SERCOS interface e. V.  
Landhausstr. 20  
D - 70190 Stuttgart, Germany  
Phone: +49(0)711-28457-50  
Fax: +49(0)711-28457-55  
E-Mail: [info@sercos.de](mailto:info@sercos.de)

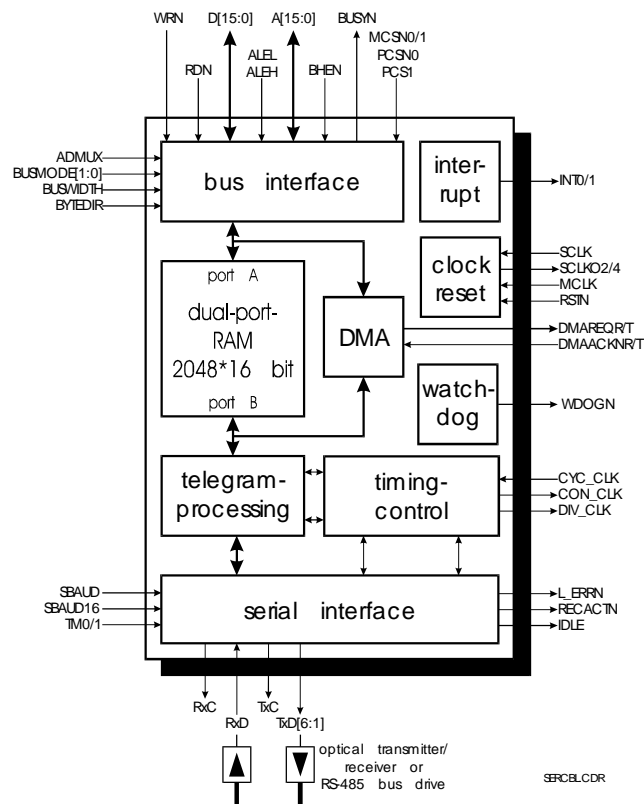


Fig. 1: SERCON816 block diagram

## SERCOS interface™ controller SERCON816

- Single-chip controller for SERCOS interface™
- Real time communication for industrial control systems
- 8/16-bit bus interface, Intel and Motorola control signals
- Dual port RAM with 2048 words \* 16-bit
- Data communications via optical fiber rings, RS 485 rings and RS 485 buses
- Maximum transmission rate of 16 Mbaud with internal clock recovery
- Internal repeater for ring connections
- Full duplex operation
- Modulation of power of optical transmitter diode
- Automatic transmission of synchronous and data telegrams in the communication cycle
- Flexible RAM configuration, communication data stored in RAM (single or double buffer) or transfer via DMA
- Synchronization by external signal
- Timing control signals
- Automatic service channel transmission
- Watchdog
- Compatible mode to SERCON410B SERCOS interface™ controller
- 100-pin plastic flat-pack casing

## A.1.1 Table of contents

A.1.1	Table of contents	6
A.1.2	Table of figures	9
<b>1</b>	<b>GENERAL DESCRIPTION</b>	<b>13</b>
<b>2</b>	<b>PIN DESCRIPTION</b>	<b>15</b>
<b>3</b>	<b>MICROPROCESSOR INTERFACE</b>	<b>19</b>
3.1	MICROPROCESSOR BUS INTERFACE	19
3.1.1	Address and data bus	19
3.1.2	Chip select signals	20
3.1.3	Bus control signals	20
3.1.4	8-bit bus mode	21
3.1.5	16-bit bus mode	22
3.1.6	Dual port RAM arbitration	22
3.2	INTERRUPTS	24
3.3	DMA INTERFACE	28
3.4	RESET AND POWER-DOWN	30
3.5	CLOCK	32
3.6	CONTROL OF DOUBLE BUFFER (VAL BIT)	32
<b>4</b>	<b>SERIAL INTERFACE</b>	<b>35</b>
4.1	CLOCK AND DATA REGENERATION	36
4.1.1	Internal clock regeneration	36
4.2	REPEATER	39
4.3	SERIAL OUTPUTS TXD1-6	40
4.4	SERIAL TRANSMITTING	41
4.5	SERIAL RECEIVING	42
4.6	TEST SIGNAL GENERATOR AND SIGNAL MONITORING	43
<b>5</b>	<b>TELEGRAM PROCESSING</b>	<b>45</b>
5.1	SERCOS INTERFACE™ PRINCIPLES	45
5.1.1	Cyclic transmission of telegrams	45
5.1.2	Telegram structure	46
5.1.3	Service channel transmission	47
5.1.4	SERCOS interface™ initialization	49
5.1.5	SERCON816 operating modes	50
5.2	SERCOS INTERFACE™ MASTER OPERATION	52
5.2.1	Timing control	52
5.2.2	Transmission of data telegrams	62
5.2.3	Service channel transmission	74
5.3	SERCOS INTERFACE™ SLAVE OPERATION	83
5.3.1	Timing control	83
5.3.2	Transmission of data telegrams	90
5.3.3	Service channel transmission	102
5.4	NON-SERCOS INTERFACE™ OPERATION	109
5.4.1	Timing control	109
5.4.2	Telegram processing	110
5.4.3	Service channel transmission	110
5.5	WATCHDOG	111
5.5.1	Watchdog enable	112
5.5.2	Trigger interval	112
5.5.3	Trigger by software	112
5.5.4	Trigger by start of MST	112
5.5.5	Watchdog interrupt	113
5.5.6	Watchdog output WDOGN	113

5.5.7	<i>Control of internal telegram processing</i>	113
<b>A</b>	<b>CONTROL REGISTERS AND RAM DATA STRUCTURES</b>	<b>115</b>
A.1	CONTROL REGISTER ADDRESSES	115
A.2	DATA STRUCTURES WITHIN THE RAM	121
A.2.1	<i>Telegram headers</i>	121
A.2.2	<i>Data containers</i>	122
A.2.3	<i>End marker</i>	123
A.2.4	<i>Service containers</i>	123
<b>B</b>	<b>PROGRAMMING EXAMPLE</b>	<b>127</b>
B.1	MASTER PROGRAMMING	127
B.1.1	<i>Control registers</i>	128
B.1.2	<i>RAM data structures</i>	129
B.1.3	<i>Service channel transmission</i>	131
B.2	SLAVE PROGRAMMING	134
B.2.1	<i>Control registers</i>	134
B.2.2	<i>RAM data structures</i>	135
B.2.3	<i>Service channel transmission</i>	137
<b>C</b>	<b>DC AND AC CHARACTERISTICS</b>	<b>142</b>
C.1	ABSOLUTE MAXIMUM RATINGS	142
C.2	RECOMMENDED OPERATING CONDITIONS	142
C.3	DC ELECTRICAL CHARACTERISTICS	142
C.4	POWER DISSIPATION	143
C.4.1	<i>Power Dissipation Considerations</i>	144
C.5	AC ELECTRICAL CHARACTERISTICS	144
C.5.1	<i>Clock input MCLK</i>	145
C.5.2	<i>Clock input SCLK</i>	145
C.5.3	<i>Address latch</i>	146
C.5.4	<i>Read access of control registers</i>	147
C.5.5	<i>Read access of dual port RAM</i>	148
C.5.6	<i>Write access to control registers</i>	149
C.5.7	<i>Write access to dual port RAM</i>	150
C.5.8	<i>BUSYN timing</i>	151
<b>D</b>	<b>MECHANICAL DATA</b>	<b>152</b>
<b>E</b>	<b>REPLACE SERCON410B BY SERCON816</b>	<b>155</b>
E.1	PINNING	155
E.2	SERIAL INTERFACE	156
E.3	REPEATER RESET MODE	157
E.4	TELEGRAM PROCESSING	157
E.4.1	<i>Speed of telegram processing</i>	157
E.4.2	<i>Bug-fix PHAS12</i>	157
E.4.3	<i>New interrupt INT_RSCEND</i>	158
E.4.4	<i>Control of double buffer (VAL bit)</i>	158
E.5	DUAL PORT RAM	159
E.6	WATCHDOG	160
E.7	CONTROL REGISTERS	160
<b>F</b>	<b>INTEGRATED CIRCUIT TEST (NANDTREE)</b>	<b>161</b>
F.1	NANDTREE USE FOR IN-CIRCUIT-TEST	161
<b>G</b>	<b>TROUBLESHOOTING</b>	<b>162</b>
G.1	DATA CORRUPTION IN CYCLIC TELEGRAM	162
G.2	MDT TELEGRAM TOO LONG	162
G.3	SPORADIC LOSS OF SERCOS IRQ	162

## A.1.2 Table of figures

Fig. 1: SERCON816 block diagram .....	3
Fig. 2: SERCON816 with ring connection (SERCOS interface™).....	11
Fig. 3: SERCON816 with RS-485 bus connection .....	11
Fig. 4: SERCON816 pin configuration .....	14
Fig. 5: Multiplexed address/data bus .....	19
Fig. 6: Chip select signals .....	20
Fig. 7: Bus control signals according to Intel standard .....	21
Fig. 8: Bus control signals according to Motorola standard .....	21
Fig. 9: Reading the dual port RAM .....	23
Fig. 10: Writing the dual port RAM .....	23
Fig. 11: Block diagram of interrupt logic .....	24
Fig. 12: DMA transfer during telegram receiving .....	28
Fig. 13: DMA transfer during DMA transmitting .....	29
Fig. 14: Clock inputs and outputs .....	32
Fig. 15: Forbidden time slot for programming VAL .....	33
Fig. 16: Serial interface with internal clock and data regeneration.....	35
Fig. 17: Data and clock regeneration .....	37
Fig. 18: Switchover between repeater and telegram .....	39
Fig. 19: Connecting the optical transmitter to TxD1-6 (TXDMODE = 0) .....	40
Fig. 20: Serial transmitter timing.....	41
Fig. 21: Serial receiver timing .....	42
Fig. 22: SERCOS interface™ communication cycle.....	45
Fig. 23: SERCOS interface™ telegram structure .....	46
Fig. 24: Write operation of service channel .....	47
Fig. 25: Read operation of service channel.....	48
Fig. 26: Telegrams during initialization .....	49
Fig. 27: Triggering of three MST cycles via falling edge of CYC_CLK .....	53
Fig. 28: Start of communication cycle too early and too late .....	56
Fig. 29: Receiving the MST by the master .....	57
Fig. 30: Telegram times.....	58
Fig. 31: Time interrupts and output signals CON_CLK and DIV_CLK .....	60
Fig. 32: DIV_CLK in mode DIVCLKMODE=1 .....	62
Fig. 33: Master data blocks.....	64
Fig. 34: Flowchart of telegram processing (master) .....	65
Fig. 35: Telegram processing in the master .....	66
Fig. 36: Processing of receive telegrams .....	67
Fig. 37: Receiving a data telegram .....	70
Fig. 38: Processing of transmit telegrams.....	72
Fig. 39: Master data telegram with data records for 4 slaves .....	73
Fig. 40: Transmitting a data telegram .....	74
Fig. 41: Automatic service channel transmission of master .....	75
Fig. 42: Service container construction .....	76
Fig. 43: Service channel write operation of master .....	79
Fig. 44: Service channel read operation of master.....	81
Fig. 45: Interrupt RSCEND .....	82
Fig. 46: Receiving the MST in the slave .....	84
Fig. 47: Receiving the MST too early .....	87
Fig. 48: Master sync telegrams missing .....	87
Fig. 49: Telegram time slots in the slave .....	88
Fig. 50: Slave data block .....	90
Fig. 51: Flowchart of telegram processing (slave).....	91
Fig. 52: Transmission blocks in the slave .....	91
Fig. 53: Processing of transmit telegrams (slave).....	94
Fig. 54: Handling of control bit FLADRMDDT .....	95

## General description

---

Fig. 55: Processing of receive telegrams (slave).....	97
Fig. 56: Receive of two data records of MDT.....	98
Fig. 57: Slave operation during phase 1 and 2 .....	99
Fig. 58: Automatic service channel transmission of slave .....	102
Fig. 59: Service container construction.....	103
Fig. 60: Service channel operation of slave.....	106
Fig. 61: Watchdog operation .....	111
Fig. 62: Watchdog trigger by MST .....	113
Fig. 63: Reset microprocessor by WDOGN.....	113
Fig. 64: Structure of data containers .....	122
Fig. 65: Structure of service container .....	123
Fig. 66: Example of service channel transmission (master).....	131
Fig. 67: Example of service channel transmission (slave) .....	137
Fig. 68: Timing of clock MCLK and related outputs .....	145
Fig. 69: Timing of clock SCLK .....	145
Fig. 70: Address latch .....	146
Fig. 71: Read access of control registers .....	147
Fig. 72: Read access of dual port RAM .....	148
Fig. 73: Write access to control registers .....	149
Fig. 74: Write access to dual port RAM.....	150
Fig. 75: BUSYN Timing .....	151
Fig. 76: PQFP-100 mechanical data.....	152
Fig. 77: Handling of control bit FLADRMDT .....	158
Fig. 78: Forbidden time slot for programming VAL.....	159
Fig. 79: Nandtree.....	161