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1 Revision history

Revision	Date	Remark
V1.0	06.04.2005	First edition
V1.1	18.04.2005	<p><u>Improvements</u></p> <ul style="list-style-type: none"> ➤ LED pin description for low-active signals LED1Port1 to LED2Port2 enhanced. ➤ More detailed description for Int_Mot pin added. <p><u>Functional Add-On's</u></p> <ul style="list-style-type: none"> ➤ New low-active signal /PHY_Reset added on pin E1, for defined reset of ethernet phy when PHYCLK output of SERCON100M is used as clock source.
V1.2	30.05.2005	<p><u>Improvements</u></p> <ul style="list-style-type: none"> ➤ Signal LED1_1 and LED1_2 renamed to /LINKPort1 and /LINKPort2.
V1.3	09.06.2005	<p>New SERCON100SL pinout added.</p> <p>Configurationpin Int_Mot eliminated</p> <p>RDY and RDYMode pin eliminated.</p>
V1.4	07.07.2005	<p>SERCON100SL</p> <ul style="list-style-type: none"> ➤ A0/BHE signal replaced by A0 ➤ New signal /BHE (/WRH) created ➤ New signal write mode WR_Mode created ➤ WR signal renamed to /WR (/WRL) ➤ PHYCLK pin eliminated <p>SERCON100M/S</p> <ul style="list-style-type: none"> ➤ DIVCLK pin added

V1.5	07.07.2005	<p>General</p> <ul style="list-style-type: none">➤ Data bus timing added➤ Power consumption added <p>SERCON100SL</p> <ul style="list-style-type: none">➤ Error on pin numbers for mode pin's M0 an M1 corrected➤ Test signal TS1 and TS2 added➤ COL1, COL2, CRS1 and CRS2 signal removed <p>SERCON100M/S</p> <ul style="list-style-type: none">➤ Test signal TS1 and TS2 added➤ COL1, COL2, CRS1 and CRS2 signal removed
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2 FPGA devices and supplement datasheets

FPGA device type	XILINX XC3S400	XILINX XC3S200
Package:	FT256 (256 ball grid)	TQ144
Databus	16/32 Bit	16 Bit
Addressbus	16 Bit	12 Bit
Ram	32 KByte	24 KByte
Master	<input type="radio"/>	<input type="checkbox"/>
Slave	<input type="radio"/>	<input type="radio"/>
Speed grade:		-4

available planned

Supplement data sheets:

Please open datasheets in a web browser -click on right mouse button and choose “open link in web-browser”.

- Introduction and ordering information
<http://direct.xilinx.com/bvdocs/publications/ds099-1.pdf>
- Functional description
<http://direct.xilinx.com/bvdocs/publications/ds099-2.pdf>
- DC and switching characteristics
<http://direct.xilinx.com/bvdocs/publications/ds099-3.pdf>
- Pinout descriptions
<http://direct.xilinx.com/bvdocs/publications/ds099-4.pdf>

Important:

Also notice device errata-sheets for additional information.

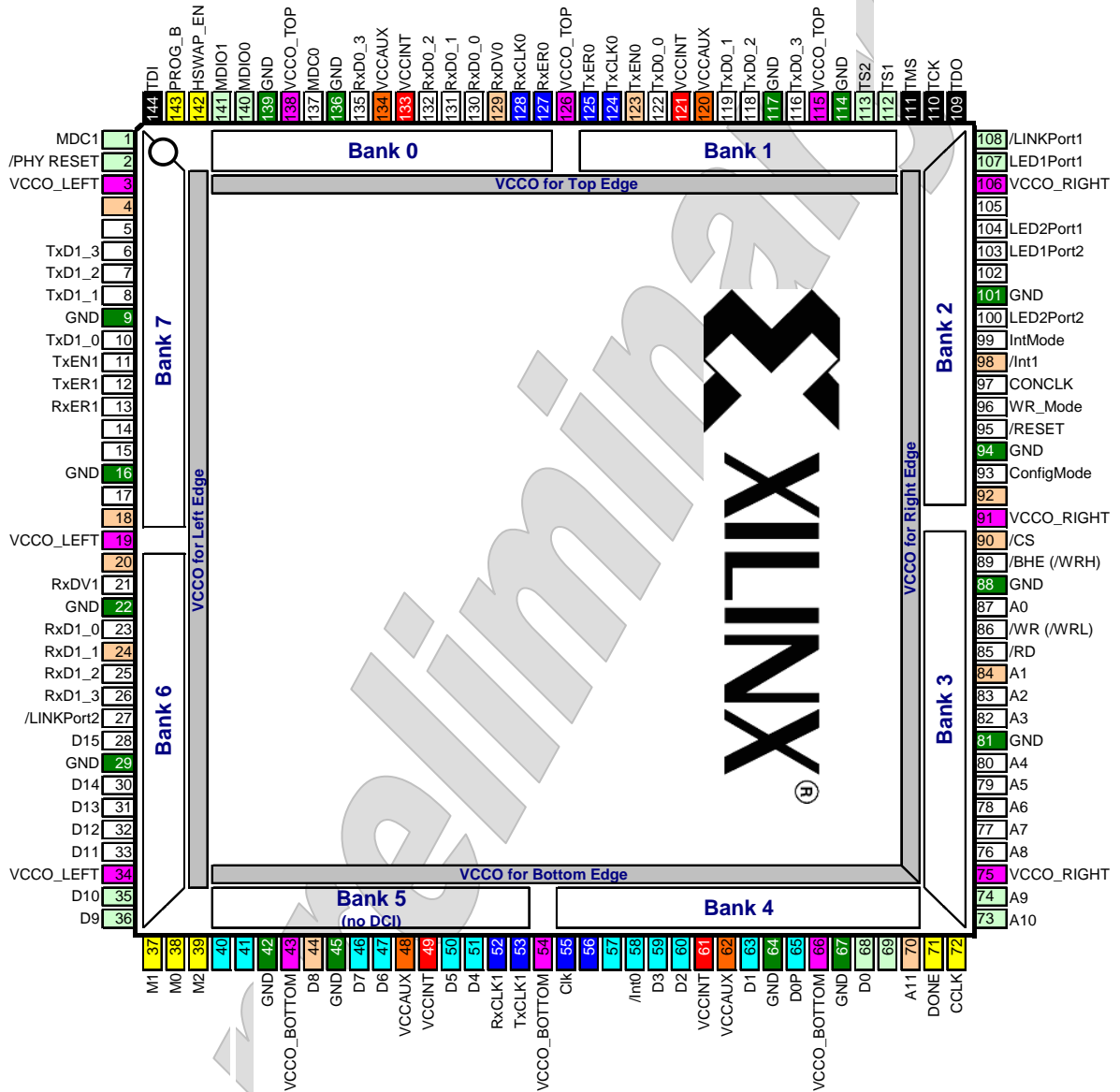
2.1 Master devices

Device	FPGA-type	Bitstream
SERCON100M-XC3S400	Xilinx XC3S400	SERCON100M_XC3S400_V1_0.bit

2.2 Slave devices

Device	FPGA-type	Bitstream
SERCON100SL-XC3S200	Xilinx XC3S200	SERCON100SL_XC3S200_V1_0.bit
SERCON100S-XC3S400	Xilinx XC3S400	SERCON100S_XC3S400_V1_0.bit

3 SERCON100SL Pinout XC3S200-TQ144 (Top view)



Signal	I/O	Location	Description	
Processor-Interface				
D15	IO	28	Data bus	
D14		30		
D13		31		
D12		32		
D11		33		
D10		35		
D9		36		
D8		44		
D7		46		
D6		47		
D5		50		
D4		51		
D3		59		
D2		60		
D1	63			
D0		68	Databusbit D0, to connect to data bus bit 0, when serial configuration mode is used, otherwise left open. ConfigMode (93) has to be set to 0V.	
D0P		65	Databusbit D0P, to connect to data bus bit 0, when parallel configuration mode is used. ConfigMode (93) has to be set to +3,3V via pullup resistor. In serial configuration mode this pin must be connected to data output of serial configuration device.	
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA

Signal	I/O	Location	Description		
A11	I	70	Addressbus		
A10		73			
A9		74			
A8		76			
A7		77			
A6		78			
A5		79			
A4		80			
A3		82			
A2		83			
A1		84			
A0		87			
/CS				90	Chip select, low-active
/WR (/WRL)				86	Write strobe, (Write strobe low), low-active
/RD				85	Read strobe, low-active
/BHE (/WRH)		89	Byte-high-enable low, (Write strobe high), low-active		
WR_Mode		96	<u>Byte write configuration</u> 0 /WR & /BHE configuration is active 1 /WRL & /WRH configuration is active		
ConfigMode		93	0 Serial configuration mode D0 (68) is used as data bus bit 0 1 Parallel configuration mode D0P (65) is used as data bus bit 0		
Global signals					
Clk	I	55	Device clock nominal 25 MHz		
/Reset	I	95	Device reset, low-active		
Test signals					
TS1	O	112	Test signal 1		
TS2	O	113	Test signal 2		
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA	

Signal	I/O	Location	Description	
Interrupts				
INT0	OD4	58	Interruptoutput 0	
INT1	OD4	98	Interruptoutput 1	
INTMode	I	99	Defines output polarity of interrupt outputs. 0 outputs low-active 1 outputs high-active	
SERCOSIII control signals				
CONCLK	O	97	CONCLK output	
Port 1 Phy signals				
RxD0_0	I	130	Receive data nibble from PHY port 1.	
RxD0_1		131		
RxD0_2		132		
RxD0_3		135		
TxD0_0	O	122	Transmitt data nibble from PHY port 1.	
TxD0_1		119		
TxD0_2		118		
TxD0_3		116		
RxDV0	I	129	Receive data valid port 1.	
RxER0	I	127	Receive error port 1.	
RxCLK0	I	128	Receive clock port 1.	
TxEN0	O	123	Transmitter enable port 1.	
TxER0	O	125	Transmitt error port 1.	
TxCLK0	I	124	Transmitt clock port 1.	
/LINKPort1	I	108	Link signal from Phy	
/LED1Port1	O8	107	Low-active LED1 of connector port 1, link information – green LED	
/LED2Port1	O8	104	Low-active LED2 of connector port 1, activity information – yellow LED	
MDIO0	I/O	140	Data signal of management interface	
MDC0	O	137	Clock signal of management interface	
PHYCLK	O		25 MHz clock signal for Phy clock distribution	
/PHYReset	O	2	Low-active reset signal for Phy	
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA

Signal	I/O	Location	Description	
Port 2 Phy signals				
RxD1_0	I	23	Receive data nibble from PHY port 2.	
RxD1_1		24		
RxD1_2		25		
RxD1_3		26		
TxD1_0	O	10	Transmitt data nibble from PHY port 2	
TxD1_1		8		
TxD1_2		7		
TxD1_3		6		
RxDV1	I	21	Receive data valid port 2.	
RxER1	I	13	Receive error port 2.	
RxCLK1	I	52	Receive clock port 2.	
TxEN1	O	11	Transmitter enable port 2.	
TxER1	O	12	Transmitt error port 2.	
TxCLK1	I	53	Transmitt clock port 2.	
/LINKPort2	I	27	Link signal from Phy	
/LED1Port2	O	103	Low-active LED1 of connector port 2, link information – green LED	
/LED2Port2	O	100	Low-active LED2 of connector port 2, activity information – yellow LED	
MDIO1	I/O	141	Data signal of management interface	
MDC1	O	1	Clock signal of management interface	
JTAG-Interface				
TDI	I	144	JTAG serial data input	
TDO	O	109	JTAG serial data output	
TCK	I	110	JTAG clock	
TMS	I	111	JTAG mode	
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA

Signal	I/O	Location	Description
Output supply voltage			
VCCO_0	Supply	3	Output supply voltage bank 0, has to be connected to $3,3V \pm 4,5\%$
VCCO_0	Supply	19	
VCCO_0	Supply	34	
VCCO_1	Supply	43	Output supply voltage bank 1, has to be connected to $3,3V \pm 4,5\%$
VCCO_1	Supply	54	
VCCO_1	Supply	66	
VCCO_2	Supply	75	Output supply voltage bank 2, has to be connected to $3,3V \pm 4,5\%$
VCCO_2	Supply	91	
VCCO_2	Supply	106	
VCCO_3	Supply	115	Output supply voltage bank 3, has to be connected to $3,3V \pm 4,5\%$
VCCO_3	Supply	126	
VCCO_3	Supply	138	
Auxiliary supply voltage			
VCCAUX	Supply	48	Auxiliary supply voltage, connect to $2,5 \pm 5\%$
VCCAUX	Supply	62	
VCCAUX	Supply	120	
VCCAUX	Supply	134	
Internal supply voltage			
VCCINT	Supply	49	Internal supply voltage, connect to $1,2V \pm 5\%$
VCCINT	Supply	61	
VCCINT	Supply	121	
VCCINT	Supply	133	

I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
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Signal	I/O	Location	Description
GND			
GND	Supply	9	Ground
GND	Supply	16	
GND	Supply	23	
GND	Supply	29	
GND	Supply	42	
GND	Supply	45	
GND	Supply	64	
GND	Supply	67	
GND	Supply	81	
GND	Supply	88	
GND	Supply	94	
GND	Supply	101	
GND	Supply	114	
GND	Supply	117	
GND	Supply	136	
GND	Supply	139	

I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
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preliminary

Configuration - Interface					
			during config	after config	n.u. not usable
M1	Config	37	I	n.u.	Configuration Mode inputs
M0	Config	38	I	n.u.	
M2	Config	39	I	n.u.	
CCLK	Config	72	I/O	n.u.	Configuration Clock
DONE	Config	71	I/O	n.u.	Done output signals errorfree configuration
PROG_B	Config	143	I	n.u.	Programm input.
HSWAP_EN	Config	142	I	n.u.	Configuration Clock
INIT_B	Config	58	I/O	INT0	Init in-/output (pin sharing with INT0)
DOUT_BUSY	Config	57	I/O	n.u.	Data out / busy
CS_B	Config	40	I	n.u.	Chip select for parallel configuration
RDWR_B	Config	41	I	n.u.	Read/write for parallel configuration

I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
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preliminary

4 SERCON100M/S Pinout XC3S400-FT256 (Top view)

		Bank 0 (Port 2)								Bank 1 (Port 1)							
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bank 7	A	GND	TDI	RxD1_1	RxD1_0	RxER1	VCCAUX	MDC1	TxCLK1	MDIO0	MDC0	VCCAUX	TxER0	TxD0_0	TxD0_2	TDO	GND
	B	RxD1_2	GND	PROG_B	RxDV1	TxER1	TxD1_3	TxD1_0	RxCLK1	GND	RxD0_3	RxD0_1	RxER0	RxDV0	TxD0_1	GND	TxD0_3
	C	RxD1_3	/LINK Port2	/LED1 Port2	HSWAP EN	TxEN1	TxD1_2	TxD1_1	MDIO1	RxCLK0	RxD0_2	RxD0_0	TxEN0	TMS	TCK	/LED1 Port1	/LINKPort1
	D	/LED2 Port2			VCCINT				PHY CLK	TxCLK0				VCCINT			/LED2 Port1
	E	/PHY RESET				VCCINT			VCCO_0	VCCO_1			VCCINT				
	F	VCCAUX					GND	VCCO_0	VCCO_0	VCCO_1	VCCO_1	GND					VCCAUX
	G						VCCO_7	GND	GND	GND	GND	VCCO_2					
	H	/Reset	GND			VCCO_7	VCCO_7	GND	GND	GND	GND	VCCO_2	VCCO_2		Config Mode	CON CLK	CYC Clk
	J	D29	D30	D31		VCCO_6	VCCO_6	GND	GND	GND	GND	VCCO_3	VCCO_3		Int1	GND	Int0
	K	D26	D27	D28			VCCO_6	GND	GND	GND	GND	VCCO_3			/WR	/CS	DIV CLK
	L	VCCAUX	D24	D25			GND	VCCO_5	VCCO_5	VCCO_4	VCCO_4	GND		Int Mode	/RD	/BE3	VCCAUX
	M	D22	D23	D16/32		VCCINT	D7			VCCO_5	VCCO_4		D0P	VCCINT	/BE2	/BE1	/BE0
	N	D19	D20	D21	VCCINT		D6			INIT_B		D1		VCCINT	A3	A2	A1
	P	D17	D18	M0	M2	D13	D9	D8		DOUT BUSY	D2		A14	A11	A7	A6	A4
	R	D16	GND	CS_B	D15	D12	D10	D5	GND		D3	A15	A13	A10	DONE	GND	A5
	T	GND	M1	RDWR_B	D14	D11	VCCAUX	D4		Clk	D0	VCCAUX	A12	A9	A8	CCLK	GND
		Bank 5								Bank 4							

Warning:

Unused pins must be left open !

Signal	I/O	Location	Description	
Processor-Interface				
D31	IO	J3	Databus	
D30		J2		
D29		J1		
D28		K3		
D27		K2		
D26		K1		
D25		L3		
D24		L2		
D23		M2		
D22		M1		
D21		N3		
D20		N2		
D19		N1		
D18		P2		
D17		P1		
D16		R1		
D15		R4		
D14		T4		
D13		P5		
D12		R5		
D11	T5			
D10	R6			
D9	P6			
D8	P7			
D7	M6			
D6	N6			
D5	R7			
D4	T7			
D3	R10			
D2	P10			
D1	N11			
D0		T10	Databusbit D0, to connect to data bus bit 0, when serial configuration mode is used, otherwise left open. ConfigMode (H14) has to be set to 0V.	
D0P		M11	Databusbit D0P, to connect to data bus bit 0, when parallel configuration mode is used. ConfigMode (H14) has to be set to +3,3V via pullup resistor. In serial configuration mode this pin must be connected to data output of serial configuration device.	
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA

Signal	I/O	Location	Description
A15	I	R11	Addressbus
A14		P12	
A13		R12	
A12		T12	
A11		P13	
A10		R13	
A9		T13	
A8		T14	
A7		P14	
A6		P15	
A5		R16	
A4		P16	
A3		N14	
A2		N15	
A1		N16	
/CS		I	
/WR	K14		Write strobe, low-active
/RD	L14		Read strobe, low-active
/BE3	L15		Byte-enable 3, low-active, defines D[31:24] to be written
/BE2	M14		Byte-enable 2, low-active, defines D[23:16] to be written
/BE1	M15		Byte-enable 1, low-active, defines D[15:8] to be written
/BE0	M16		Byte-enable 0, low-active, defines D[7:0] to be written
D16_32	I	M3	Defines databuswidth 0 databuswidth 16 bit 1 databuswidth 32 bit
ConfigMode	I	H14	0 Serial configuration mode D0 (T10) is used as data bus bit 0 1 Parallel configuration mode D0P (M11) is used as data bus bit 0
Global signals			
Clk	I	T9	Device clock nominal 25 MHz
/Reset	I	H1	Device reset, low-active
Test signals			
TS1	O	M13	Test signal 1
TS2	O	H3	Test signal 2

I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
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Signal	I/O	Location	Description
Interrupts			
INT0	O	J16	Interruptoutput 0
INT1	O	J14	Interruptoutput 1
INTMode	I	L13	Defines output polarity of interrupt outputs. 0 outputs low-active 1 outputs high-active
SERCOSIII control signals			
CONCLK	O	H15	CONCLK output
CYCCLK	I	H16	CYCCLK input
DIVCLK	O	K16	DIVCLK output
Port 1 Phy signals			
RxD0_0	I	C11	Receive data nibble from PHY port 1.
RxD0_1		B11	
RxD0_2		C10	
RxD0_3		B10	
TxD0_0	O	A13	Transmitt data nibble from PHY port 1.
TxD0_1		B14	
TxD0_2		A14	
TxD0_3		B16	
RxDV0	I	B13	Receive data valid port 1.
RxER0	I	B12	Receive error port 1.
RxCLK0	I	C9	Receive clock port 1.
TxEN0	O	C12	Transmitter enable port 1.
TxER0	O	A12	Transmitt error port 1.
TxCLK0	I	D9	Transmitt clock port 1.
/LINKPort1	I	C16	Link signal from Phy
/LED1Port1	O8	C15	Low-active LED1 of connector port 1, link information – green LED
/LED2Port1	O8	D16	Low-active LED2 of connector port 1, activity information – yellow LED
MDIO0	I/O	A9	Data signal of management interface
MDC0	O	A10	Clock signal of management interface
PHYCLK	O	D8	25 MHz clock signal for Phy clock distribution
/PHYReset	O	E1	Low-active reset signal for Phy

I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
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Signal	I/O	Location	Description	
Port 2 Phy signals				
RxD1_0	I	A4	Receive data nibble from PHY port 2.	
RxD1_1		A3		
RxD1_2		B1		
RxD1_3		C1		
TxD1_0	O	B7	Transmitt data nibble from PHY port 2	
TxD1_1		C7		
TxD1_2		C6		
TxD1_3		B6		
RxDV1	I	B4	Receive data valid port 2.	
RxER1	I	A5	Receive error port 2.	
RxCLK1	I	B8	Receive clock port 2.	
TxEN1	O	C5	Transmitter enable port 2.	
TxER1	O	B5	Transmitt error port 2.	
TxCLK1	I	A8	Transmitt clock port 2.	
/LINKPort2	I	C2	Link signal from Phy	
/LED1Port2	O	C3	Low-active LED1 of connector port 2, link information – green LED	
/LED2Port2	O	D1	Low-active LED2 of connector port 2, activity information – yellow LED	
MDIO1	I/O	C8	Data signal of management interface	
MDC1	O	A7	Clock signal of management interface	
JTAG-Interface				
TDI	I	A2	JTAG serial data input	
TDO	O	A15	JTAG serial data output	
TCK	I	C14	JTAG clock	
TMS	I	C13	JTAG mode	
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA

Signal	I/O	Location	Description	
Output supply voltage				
VCCO_0	Supply	E8	Output supply voltage bank 0, has to be connected to $3,3V \pm 4,5\%$	
VCCO_0	Supply	F7		
VCCO_0	Supply	F8		
VCCO_1	Supply	E9	Output supply voltage bank 1, has to be connected to $3,3V \pm 4,5\%$	
VCCO_1	Supply	F9		
VCCO_1	Supply	F10		
VCCO_2	Supply	G11	Output supply voltage bank 2, has to be connected to $3,3V \pm 4,5\%$	
VCCO_2	Supply	H11		
VCCO_2	Supply	H12		
VCCO_3	Supply	J11	Output supply voltage bank 3, has to be connected to $3,3V \pm 4,5\%$	
VCCO_3	Supply	J12		
VCCO_3	Supply	K11		
VCCO_4	Supply	L9	Output supply voltage bank 4, has to be connected to $3,3V \pm 4,5\%$	
VCCO_4	Supply	L10		
VCCO_4	Supply	M9		
VCCO_5	Supply	L7	Output supply voltage bank 5, has to be connected to $3,3V \pm 4,5\%$	
VCCO_5	Supply	L8		
VCCO_5	Supply	M8		
VCCO_6	Supply	J5	Output supply voltage bank 6, has to be connected to $3,3V \pm 4,5\%$	
VCCO_6	Supply	J6		
VCCO_6	Supply	K6		
VCCO_7	Supply	G6	Output supply voltage bank 7, has to be connected to $3,3V \pm 4,5\%$	
VCCO_7	Supply	H5		
VCCO_7	Supply	H6		
I Input		O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA

Signal	I/O	Location	Description				
Auxiliary supply voltage							
VCCAUX	Supply	A6	Auxiliary supply voltage, connect to $2,5 \pm 5\%$				
VCCAUX	Supply	A11					
VCCAUX	Supply	F1					
VCCAUX	Supply	F16					
VCCAUX	Supply	L1					
VCCAUX	Supply	L16					
VCCAUX	Supply	T6					
VCCAUX	Supply	T11					
Internal supply voltage							
VCCINT	Supply	D4	Internal supply voltage, connect to $1,2V \pm 5\%$				
VCCINT	Supply	D13					
VCCINT	Supply	E5					
VCCINT	Supply	E12					
VCCINT	Supply	M5					
VCCINT	Supply	M12					
VCCINT	Supply	N4					
VCCINT	Supply	N13					
Signal	I/O	Location					
GND							
GND	Supply	A1	Ground				
GND	Supply	A16					
GND	Supply	B2					
GND	Supply	B9					
GND	Supply	B15					
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">I Input</td> <td style="width: 25%;">O output push-pull 2mA</td> <td style="width: 25%;">OD4 open-drain 4 mA</td> <td style="width: 25%;">O8 output push-pull 8 mA</td> </tr> </table>				I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA				

Signal	I/O	Location	Description
GND			
GND	Supply	F6	
GND	Supply	F11	
GND	Supply	G7	
GND	Supply	G8	
GND	Supply	G9	
GND	Supply	G10	
GND	Supply	H2	
GND	Supply	H7	
GND	Supply	H8	
GND	Supply	H9	
GND	Supply	H10	
GND	Supply	J7	
GND	Supply	J8	
GND	Supply	J9	
GND	Supply	J10	
GND	Supply	J15	
GND	Supply	K7	
GND	Supply	K8	
GND	Supply	K9	
GND	Supply	K10	
GND	Supply	L6	
GND	Supply	L11	
GND	Supply	R2	
GND	Supply	R8	
GND	Supply	R15	
GND	Supply	T1	
GND	Supply	T16	

I Input	O output push-pull 2mA	OD4 open-drain 4 mA	O8 output push-pull 8 mA
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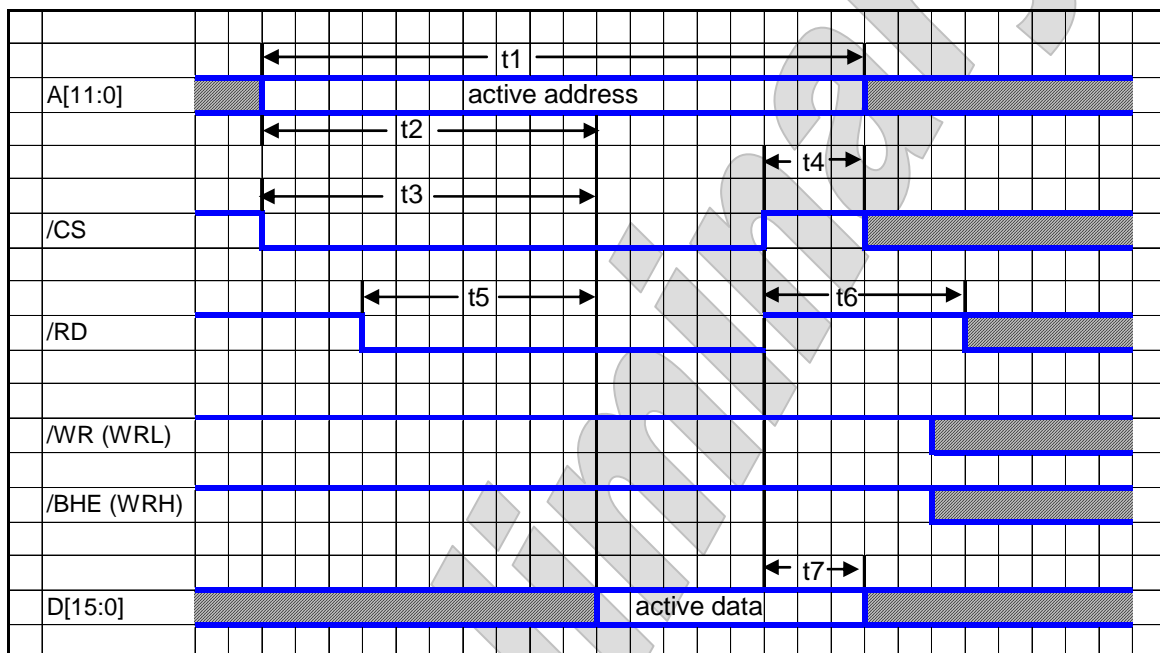
Signal	I/O	Location	Description		
Configuration - Interface					
			during config	after config	n.u. not usable
M0	Config	P3	I	n.u.	Configuration Mode inputs
M1	Config	T2	I	n.u.	
M2	Config	P4	I	n.u.	
CCLK	Config	T15	I/O	n.u.	Configuration Clock
DONE	Config	R14	I/O	n.u.	Done output signals errorfree configuration
PROG_B	Config	B3	I	n.u.	Programm input.
HSWAP_EN	Config	C4	I	n.u.	Configuration Clock
INIT_B	Config	N9	I/O	I/O	Init in-/output
DOUT_BUSY	Config	P9	I/O	I/O	Data out / busy
CS_B	Config	R3	I	I/O	Chip select for parallel configuration
RDWR_B	Config	T3	I	I/O	Read/write for parallel configuration
I Input		O output push-pull 2mA		OD4 open-drain 4 mA	O8 output push-pull 8 mA

5 Electrical characteristics

5.1 Timing

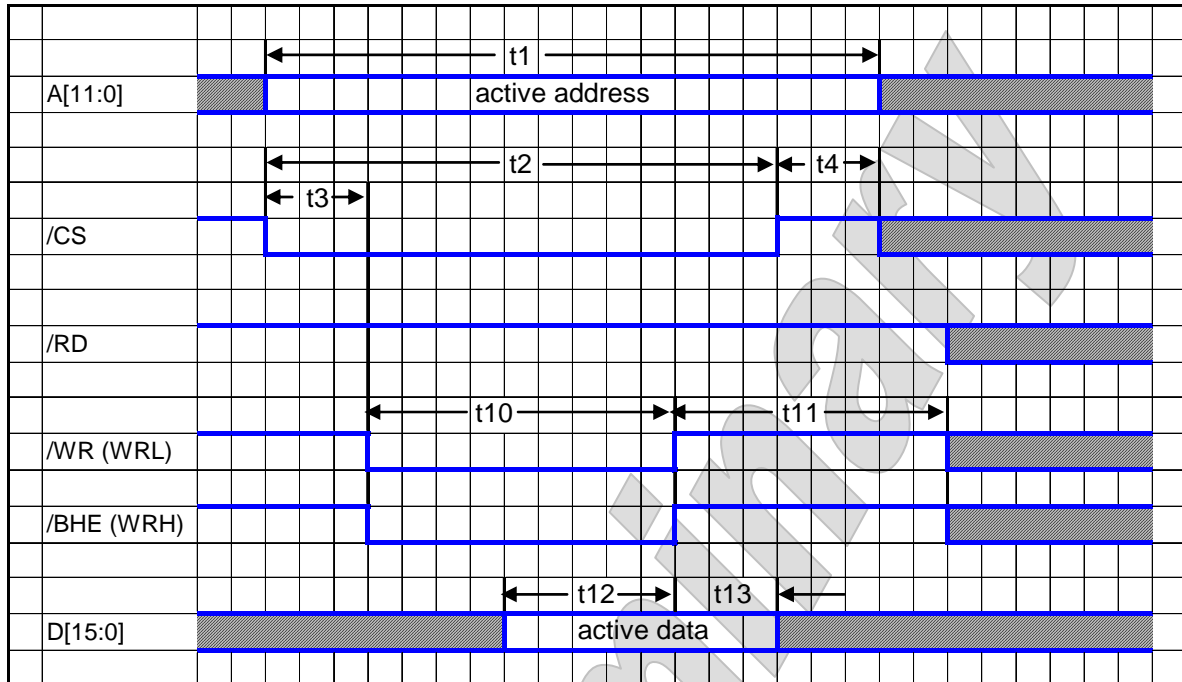
5.1.1 SERCON100SL

5.1.1.1 Read access



Time	Description	Min.	Typ.	Max.
t1	Cycle time	100 ns		
t2	Address to valid data			60 ns
t3	/CS to driven data			30 ns
t4	/CS high time	20 ns		
t5	/RD to driven data			30 ns
t6	/RD high time	35 ns		
t7	Data hold after positive edge of /RD or /CS whatever is first	10 ns		20 ns

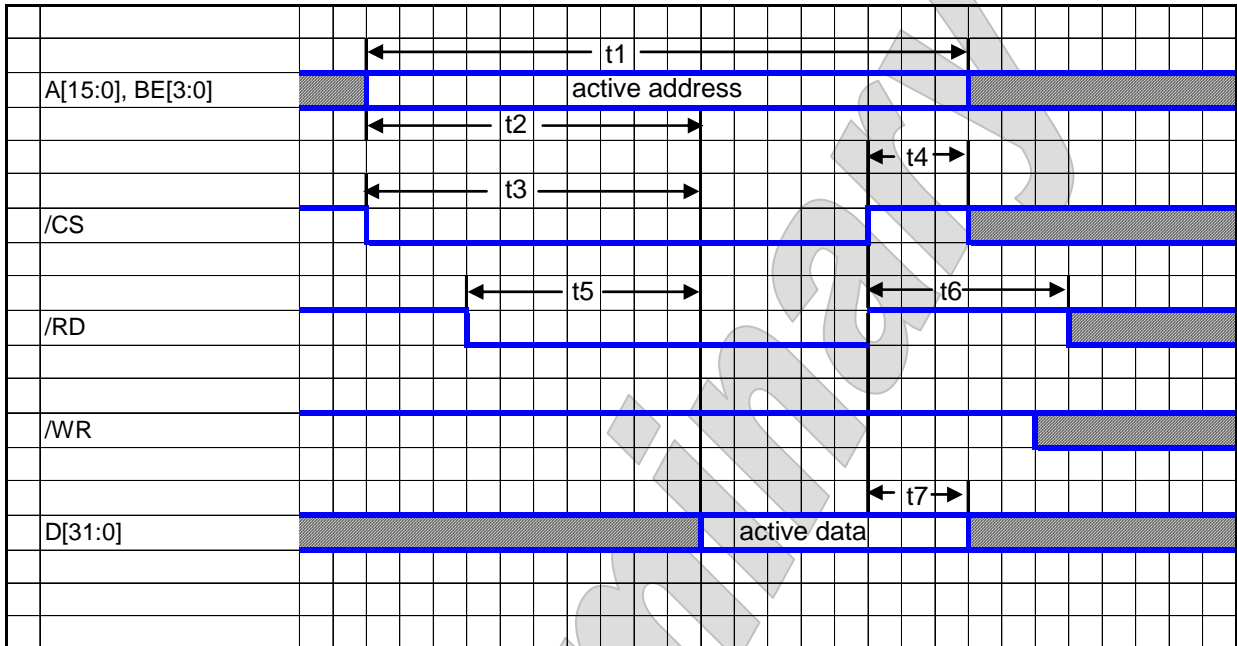
5.1.1.2 Write access



Time	Description	Min.	Typ.	Max.
t1	Cycle time	100 ns		
t2	Chip select low time	80 ns		
t3	/CS low to /WR, /BHE low	0 ns		
t4	/CS high	20 ns		
t10	/WR, /BHE low time	80 ns		
t11	/WR, /BHE high time	20 ns		
t12	Data valid before positive edge of /WR, /BHE	40 ns		
t13	Data hold after positive edge of /WR, /BHE	0 ns		

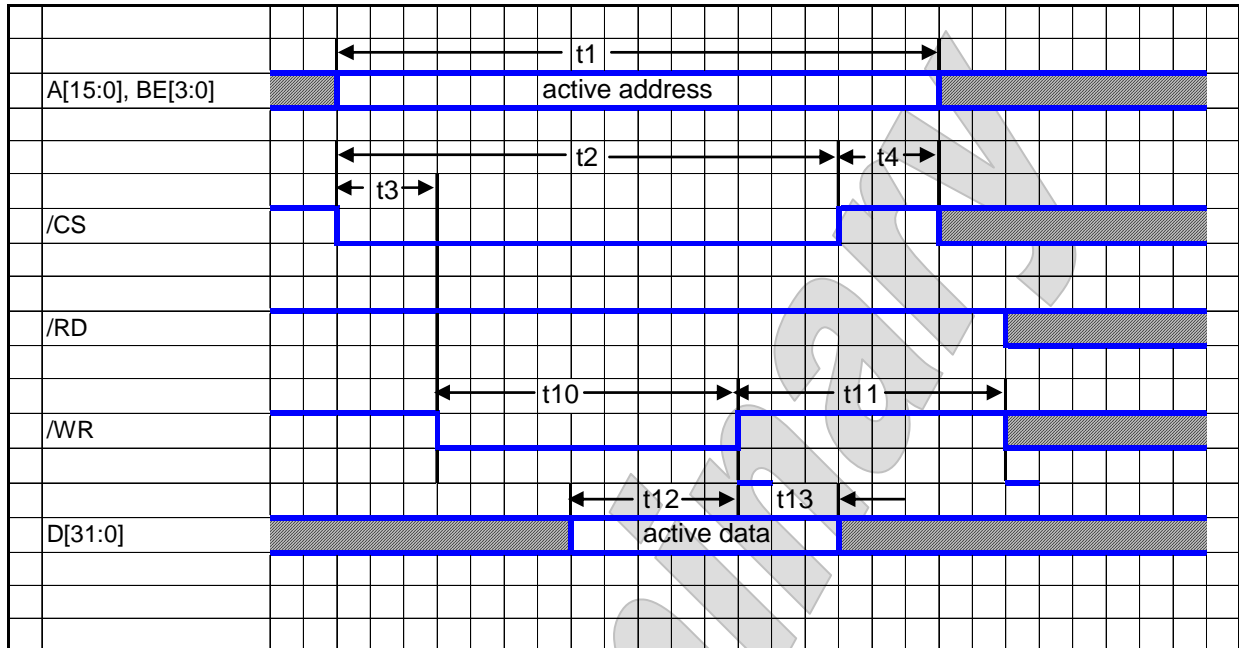
5.1.2 SERCON100M/S

5.1.2.1 Read access



Time	Description	Min.	Typ.	Max.
t1	Cycle time	100 ns		
t2	Address to valid data			60 ns
t3	/CS to driven data			30 ns
t4	/CS high time	20 ns		
t5	/RD to driven data			30 ns
t6	/RD high time	35 ns		
t7	Data hold after positive edge of /RD or /CS whatever is first	10 ns		20 ns

5.1.2.2 Write access



Time	Description	Min.	Typ.	Max.
t1	Cycle time	100 ns		
t2	Chip select low time	80 ns		
t3	/CS low to /WR low	0 ns		
t4	/CS high	20 ns		
t10	/WR low time	80 ns		
t11	/WR high time	20 ns		
t12	Data valid before positive edge of /WR	40 ns		
t13	Data hold after positive edge of /WR	0 ns		

6 Available configuration modes

Configuration Mode	M0	M1	M2	Synchronizing Clock	Data Width	Serial DOUT
Master Serial	0	0	0	CCLK Output	1	Yes
Slave Serial	1	1	1	CCLK Input	1	Yes
Slave Parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

preliminary

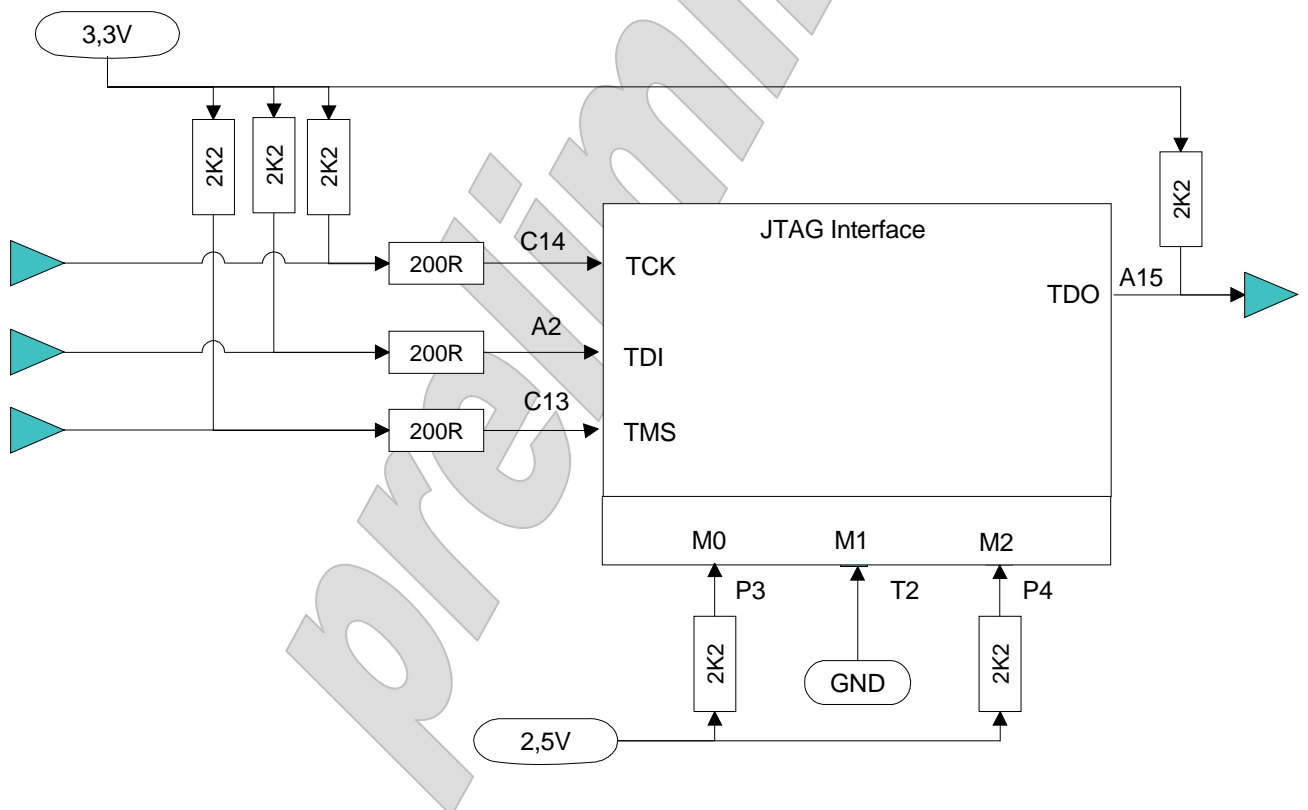
Remark:

Care must be taken designing the configuration interface. The signals

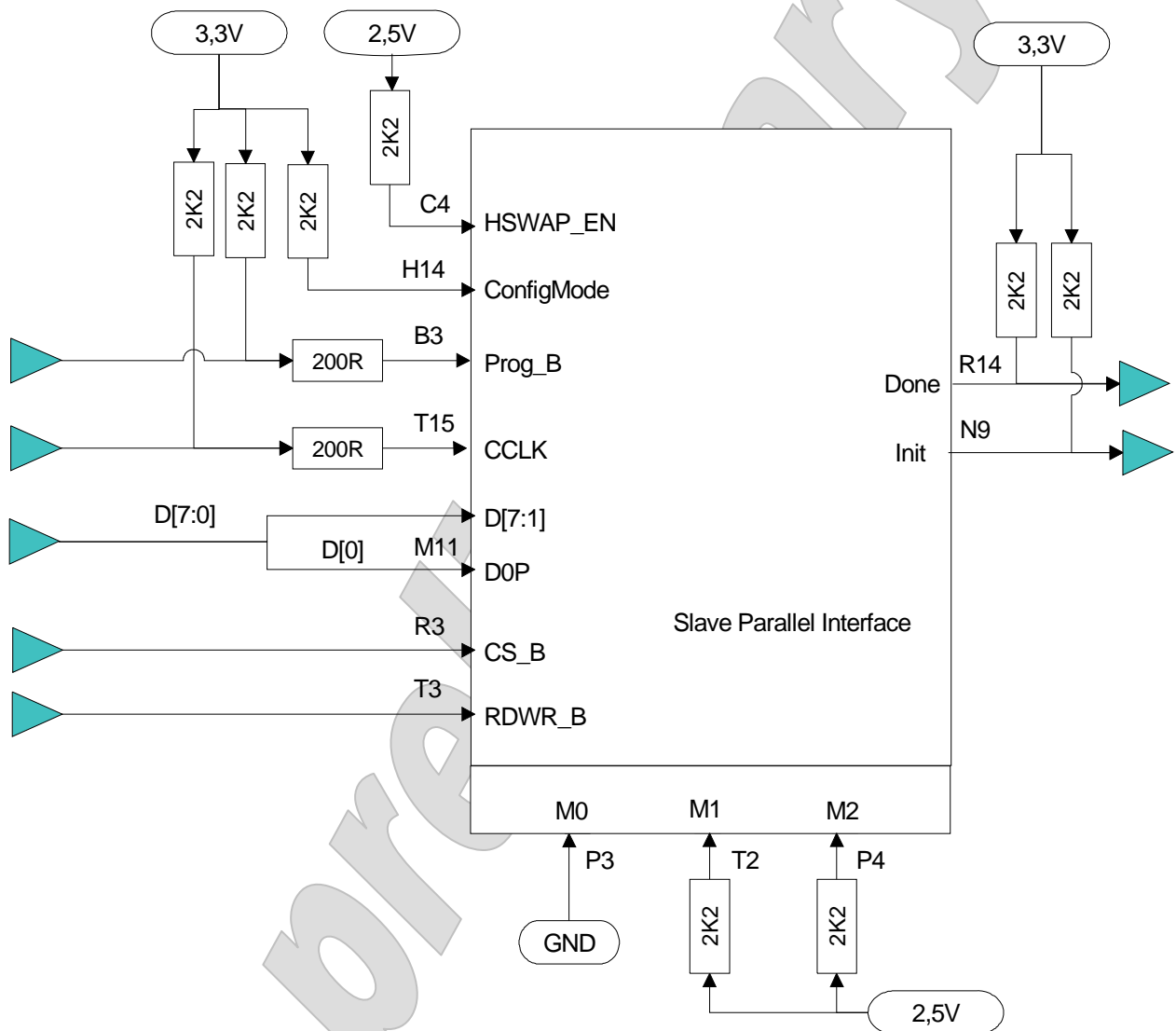
- M0, M1, M2
- CCLK
- PROG_B
- DONE
- HSWAP_EN
- and the JTAG interface TDI, TMS, TCK, TDO

are only 2.5V compliant. For controlling the input current are series input resistor or resistor –divider is needed.

- JTAG Configuration



- Slave Parallel Mode:



- Master Serial Mode:

