SERCON816

Specification

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1.0	4/12/1998	Proposal
1.1	17/12/1998	1. Revision
1.2	15/03/1999	2. Revision / Update of implemented changes
1.3	11/5/1999	Document of Work, Bitrate

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FIGURES

1 Overview

1.1 Introduction

The new SERCON816 ASIC is the next generation of SERCON interface controller following the SERON410B. The goal was to develop an ASIC to be down compatible with the existing SERCON410B but to offer essentially enhanced features. The SERCON410B ASIC is manufactured in the 0.7µm HCMOS technology, where as the new SERCON816 ASIC is manufactured in the 0.5µm/5V HCMOS technology of STMicroelectronics.

Aside of transferring the technology, following enhancements of features and functions are implemented as well:

- Increase of serial transmission rate from 2 and 4 MBit/s to 2, 4, 8 and 16 MBit/s. External clock generation is not necessary anymore. Speed of parallel data processing (telegram processing) is increased accordingly.
- Double internal Dual Port RAM (DPRAM) from 1K words to 2K words
- Introduction of Watchdog to monitor software and external synchronization signals.
- Reset value for Repeater Mode of the serial interface is configurable through input pins.
- New Mode of output DIV_CLK

Using the SERCON410B, some irregular behavior can be observed in some operating modes, which limits the usage ability. Following errors will be corrected in the new SERCON816.

- *Specification of BUSY signal*
  The timing of this signal is described in a wrong way in the actual specification. The new data sheet for the SERCON816 will be modified accordingly.
- *Constantly sending of drive data telegrams (AT) during phase 1 and 2:*
  if a drive is requested to send AT's, this will not be done once, but repeated constantly.
- *Asynchronous Access to DPR*:
  if data are written at any time during the transmission cycle into the Dual Port RAM via the bus interface, it can happen, that these data are been over written by the internal telegram processing. This issue will not be solved generally. Instead of this a work around will be implemented for two types of data that turned out to be the most critical is real applications.

1.2 Cross Reference

This delta specification is based on following documents:

- SERCON410B Reference Manual (08/93)
- Protocol of Meeting at ST on 17.11.98
- Extended offer by 5.3.99

2 Specification SERCON816

Following a description of the new SERCON816 is given. Only those item are listed that are different or additional to the actual SERCON410B.

2.1 Technology

The ASIC is manufactured in the 0.5µm/5V HCMOS5 technology of STMicroelectronics.

2.2 Pinning

The ASIC is available in QFP100 and TQFP100 package. Aside of some differences both the SERCON816 and the SERCON410B offer the same functionality. Due to the extended functionality it has been necessary to redefine some of SERCON410B chip to accomplish the new features. The remaining pins have the same function as present.

No.	SERCON410B	SERCON816	Function SERCON816
28	SREGEN	SBAUD16	Bit rate serial Interface (together with SBAUD) and compatibility mode SERCON410B: 0: 8, 16 MBit/s 1: 2, 4 MBit/s
24	TxDNRZ	WDOGN	Watchdog Output 0: Watchdog-Output active 1: Watchdog-Output not active
13	TxC (I/O)	TxC (O)	Output for Transmit Clock
12	RxC (I/O)	RxC (O)	Output for regenerated Receive Clock

2.3 Serial Interface

The SERCON816 serial interface transmits and receives data from the serial data stream. Data and clock rate of the data stream are regenerated using the incoming serial data. The SERCON410B offers the capability to recover the 'bit clock' using an external circuitry and to feed to data and clock separately to the chip. This is not available for the SERCON816. Due to the fact, in the new chip the internal clock recovery can handle high bit rates, this external circuitry is not needed any more.

2.3.1 Serial Clock (SCLK)

Clock recovery is done by a state machine (DPLL_FSM), which is clocked with a clock which is 16 times the frequency of the incoming bit rate. In case the bit rate is 16Mbit/s, a clock frequency of 256MHz is resulting for the DPLL_FSM. This frequency is generated by multiplying 4 time the clock at input SCLK. Like for the SERCON410B the frequency for SCLK is set to be 64MHz. Increase of frequency is achieved by using an analog PLL according to the PLL51 macro.

As a result the DPLL_FSM generates a clock signal which is according to the used bit rate of either 2, 4, 8 or 16 MHz. This is the input clock for the serial receiver and transmitter.

The chosen bit rate can be defined by pins or software. Due to this new feature a new pin (SBAUD16) and control bit (SWBAUD16) is introduced.

Bit rate for SCLK = 64 MHz					
ENTSBAUD (Addr. 1H.10)	**SBAUD (Pin 29)**	**SBAUD16 (Pin 28)**	**SWBAUD (Addr. 1H.6)**	**SWBAUD16 (Addr. 1H.15)**	**Bit rate**
0	1	1	X	X	2 MBit/s
0	0	1	X	X	4 MBit/s
1	x	1	1	X	2 MBit/s
1	x	1	0	X	4 MBit/s
0	1	0	X	X	8 MBit/s
0	0	0	X	X	16 MBit/s
1	x	0	1	1	2 MBit/s
1	x	0	0	1	4 MBit/s
1	x	0	1	0	8 MBit/s
1	x	0	0	0	16 MBit/s

In addition the clock outputs SCLKO2 and SCLKO4 are controlled by pin SBAUD16:

SCLKO2, SCLKO4 for SCLK = 64 MHz		
SBAUD16	**SCLKO2**	**SCLKO4**
1	32 MHz	16 MHz
0	64 MHz	32 MHz

2.3.2 SERCON410B Compatible Mode

SERCON410B application using internal clock recovery have the pin SREGEN (new SBAUD16) tied to logic high = ‘1’ level. Using this, the new SERCON816 is forced to operate in it’s compatible mode.

Using this mode, only two bit rates, 2 and 4 Mbit/s are selectable and at pins SCLKO2 and SCLKO4 the same frequencies as for the SERCON410B are available.

To be able to use the new available bit rates, pin SBAUD16 must be tied to logic level ‘0’.

2.3.3 Repeater

The repeater for the serial interface is switched on '1' and off '0' through the control bit REPON. The reset value of the control bit can be determined by the pins TM0-1:

TM0	TM1	REPON after Reset (Address 1H.3)	Test mode
1	1	1: Repeater on	None
0	0	0: Repeater off	None
0	1	1	TxD1-6 continues signal light
1	0	1	Zero bit stream

Configuration of pins TM0-1 determines REPON only during reset phase of the chip. Thereafter TM0-1 have no influence on the content of REPON.

The control bits TMODE2-0 can also over write the actual test mode. Coding for this control bits does not change. TMODE2-0 has no influence to REPON.

2.4 Telegram Processing

2.4.1 Clock for Telegram Processing (MCLK)

Except the serial interface the telegram processing unit and all other part of the circuitry are clocked by MCLK. The faster serial transmission rate requires a faster processing of data and therefore a faster clock MCLK. A maximum clock frequency of 32MHz for MCLK can be granted by technology, target frequency is 64MHz.

2.5 Dual Port RAM

The internal Dual Port RAM is extended from 1024 x 16 Bit (SERCON410B) up to 2048 x 16 Bit (SERCON816). Due to this the addressing of the DPR and control register via the bus interface changes.

The internal DPR is addressed through the address pins A11-A1 and the chip select inputs MCSN0-1. The internal control register are selected via the chip select inputs PCSN0 and PCS1. Existing SERCON410B systems might have the address pin A11 connected to the chip select inputs MCSN1 and PCS1 in order to distinguish between RAM and control registers. Using the new SERCON816, address bit A12 must be used for this. When using the SERCON816 in an existing application, the upper range of 1024 words can not be used.

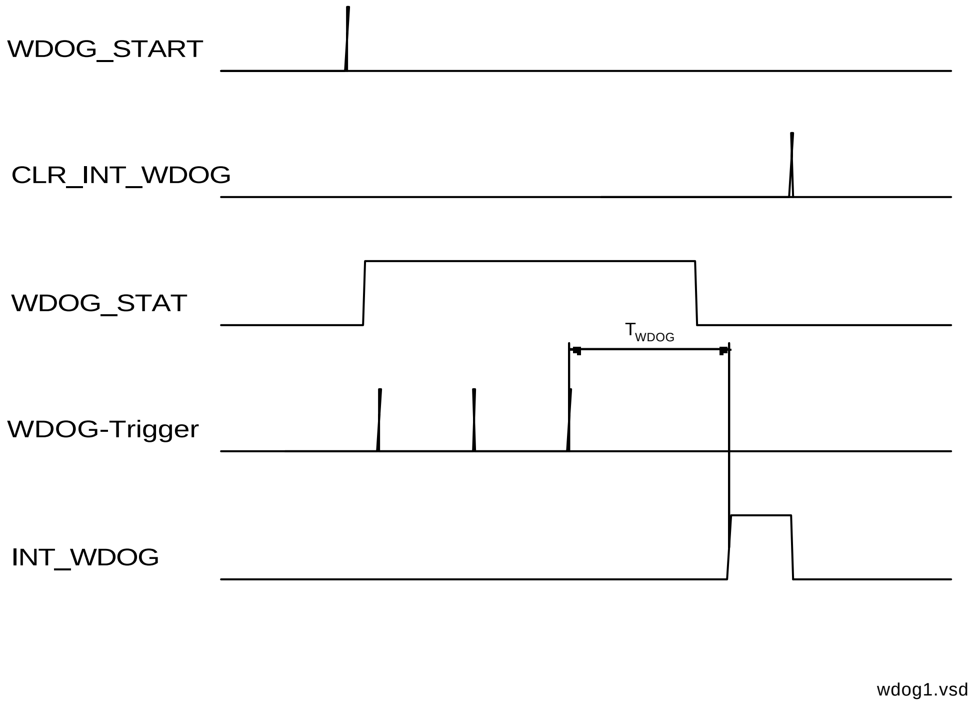
In this case, when the upper range of 1K words of the RAM is not usable by the bus interface, the address pointers in the telegram headers have to be programmed so that this upper region can not be used by the telegram processor.

2.6 Watchdog

The watchdog of the SERCON816 is used for monitoring the input signal CYC_CLK and software functions.

For monitoring, the watchdog must be triggered regularly during a programmable interval. In case the trigger fails, the watchdog goes active. When the watchdog is active, the interrupt flag INT_WDOG is set. This interrupt has two possible enable bits, like all other interrupts have, for the interrupt outputs INT0 and INT1 (Enx_INT_WDOG) and one control bit for clearing the interrupt flag (CLR_INT_WDOG).

After chip reset the watchdog is OFF, but can be activated by writing the control bit WDOG_START. Once activated, not switch off is possible except by software reset If the watchdog activates, it switches off automatically. The watchdog interrupt remains set until it is cleared by a reset or writing to CLR_INT_WDOG. The actual status of the watchdog is register in status bit WDOG_STAT.



EINBETTENFORMATVERBINDENEINBETTEN***Figure 1: Watchdog Interrupt***

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2.6.1 Watchdog Output WDOGN

The interrupt flag INT_WDOG also can activate the watchdog output WDOGN in addition. This must be enabled through the control bit WDOUT_EN. The output WDOGN is an active '0' signal which can be connected to the reset input of the controlling micro processor. In order to enable a reset of the micro processor, the signal WDOGN is reset after time T_{WDOUT}. After booting, the micro processor can determine if the reset happened through the watchdog or a power-on-reset by reading the watchdog interrupt flag INT_WDOG.

The active time for WDOGN is approximately 2 to 3 µsec. Time 1µsec is given by divider MCLKDIV. Watchdog output then remains active for the next minimum 2, maximum 3 periods of this divider.

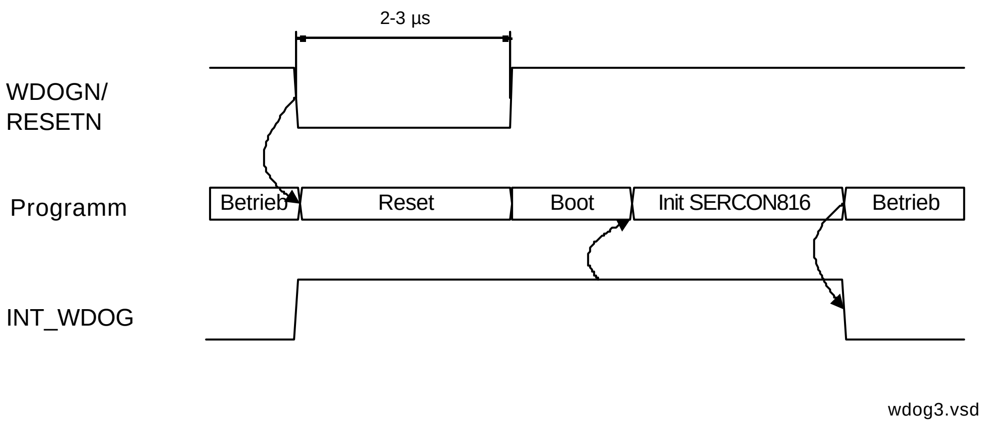

Figure 2: Reset Processor via Output WDOGN

2.6.2 Watchdog Influence to Telegram Processing

Activation of the watchdog (INT_WDOG=1) sets internal registers of the SERCON816.

Register	RESET value by INT_WDOG=1
ENTMT (Addr.3H.8)	0
PHAS0 (Addr.AH.0-7)	0H

Register bit ENTMT enables transmission of telegrams (Master- and Slave-Mode). By reset of ENTMT transmission of AT's (Slaves) and MDT's (Master) will be suppressed after the watchdog is active.

In register PHAS0 phase information is determined , which the SERCON816 is transmitting when sending an MST (Master-Mode) . After reset of this register the SERCON816 transmits MST's of phase 0 after watchdog is active.

These register bits can be programmed again by the bus interface only after the status bit INT_WDOG is cleared.

Reset of these control bits through hardware, respectively software reset has higher priority than reset through INT_WDOG!

2.6.3 Trigger Interval

The trigger Interval is determined by the divider MCLKDIV and the value of TWDOG15-0.

$$T_{WDOG} = \frac{(MCLKDIV + 1) \bullet TWDOG}{f_{MCLK}}$$

After the watchdog is enabled, an internal down counter is preset with the value of TWDOG. The counter then counts with the given frequency of MCLKDIV, which typically is 1µsec. Reaching the counter value 0000H, the watchdog is set. Each trigger even again loads the counter to the value of TWDOG.

2.6.4 Trigger by Software

The watchdog also can be triggered by software. This is possible by writing the value 42H to the control bits WDOG_TRIG (29H,7-0).

Triggering by writing the control bits WDOG_TRIG is possible at any time.

2.6.5 Trigger by CYC_CLK

Being set to master mode, the input CYC_CLK is synchronizing the start of one or more SERCOS cycles. The SERCON816 is able to watch if the input signal CYC_CLK is repeated during a programmable time window (JTSCYC1, JTSCYC2). If the signal CYC_CLK is not inside this window, the interrupt MSTEARLY goes active. If there no input signal CYC_CLK at all, this interrupt will not be set. The watchdog is an additional control of the input signal CYC_CLK

The watchdog is not triggered directly with the signal CYC_CLK, but by the start signal for the MST's caused by CYC_CLK. If the input CYC_CLK fails, the watchdog goes active after a certain time interval after start of the last MST.

This mode is possible only when operating in master mode. Triggering with the internal MST start signal must be enabled through the control bit WDOG_MSTEN.

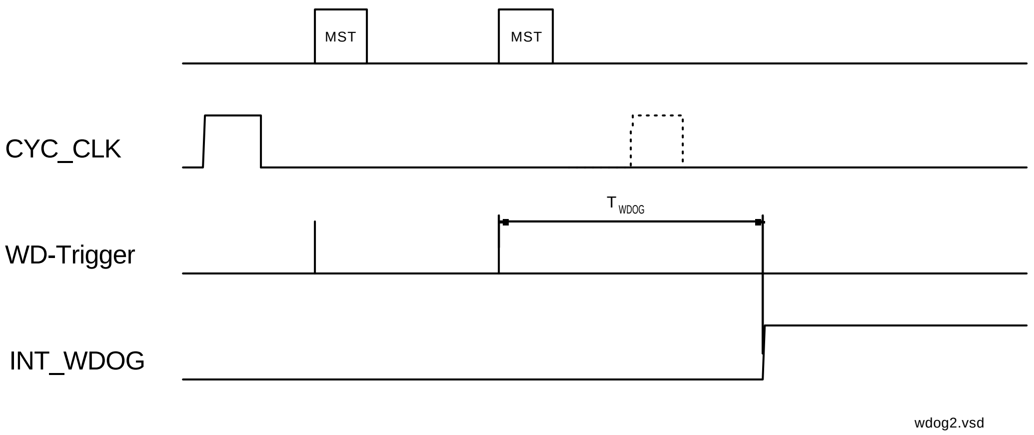

Figure 3: Watchdog Trigger with MST

2.7 Output DIV_CLK

In the SERCON410B the output DIV_CLK becomes active several time during one SERCOS cycle. The first point in time for an active output is programmed by the control register TDIVCLK (1EH). The distance between two pulses of DIV_CLK is determined by register DTDIVCLK (1FH). The active level of the output is set by register POLDIVCLK (20H,8) and the number of pulses during one SERCOS cycle is set by register NDIVCLK (20H,7-0).

SERCON816 has a new mode for the output DIV_CLK. This can be selected with the new control bit DIVCLKMODE. In this mode the output DIV_CLK will not active multiple time during a SERCOS cycle, but only once after a programmable amount of SERCOS cycles.

DIVCLKMODE (20H.9)	**Function**
0	Multiple during one cycle (as for SERCON410B)
1	One time during multiple SERCOS cycles

The value of DIVCLKMODE after reset is ‘0’. Due to this the behavior of the SERCON816 is the same as for the SERCON410B.

The amount of SERCOS cycles when the output DIV_VLK becomes active is determined with the control bit NDIVCLK.

NDIVCLK (10H.7-0)	**Function DIV_CLK**
0	Never becomes active
1	Active once in each cycle
2	Active after each second cycle
3	Active after each third cycle
N	Active after each N-th cycle.

The output DIV_CLK goes active the first time in the first SERCOS cycle (if NDIVCLK != 0) or after the first cycle when NDIVCLK is being programmed to a value not equal zero.

The control register TDIVCLK determines the point in time in a SERCOS cycle when DIV_CLK becomes active. This is equivalent to the first timing point of the former DIV_CLK mode. Polarity and length of DIV_CLK remain unchanged with respect to the old mode.

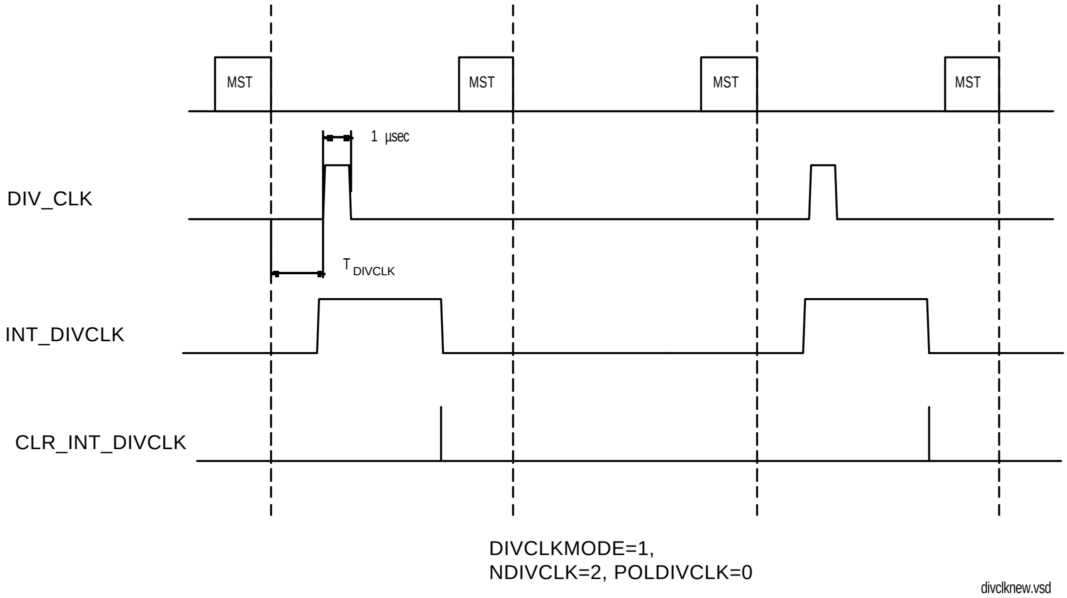

Figure 4: New Mode DIV_CLK

2.8 Bug Fix „Specification BUSY-Signal“

The output BUSYN of the micro processor bus interface has to have a maximum length of one cycle of MCLK. Evaluation during measurements have shown that the length of BUSYN can be much longer. The logic for generating the BUSY signal will be checked to determine the reasons for the long BUSY times. The maximum BUSY time has to be defined again for the new specification.

2.9 Bug Fix „Phase 1,2 Error“

2.9.1 Error Description

During the communication phases 1 and 2 the drive (SERCON in Slave Mode) should send an telegram only in case it is requested to do so by the master. After the request the telegram should be send only once. The SERCON410B is constantly sending the telegram until the master is requesting another drive to send the telegram.

2.9.2 Reason and Fix of Error

The above described behavior is controlled through an SERCOS410B internal flag (FLMDTADR, 25H, 12). This flag is set when the corresponding address is determined in the received telegram. If the flag is set, the drive telegram (AT) is send during the next transmission cycle. In the SERCON410B the flag (FLMDTADR) is reset only after a new MDT is received including a different address than the expected one. A missing MDT does not reset the flag causing AT's to be send multiple times.

In the SERCON816, the flag FLMDTADR is reset after starting to send a telegram when initiated when the flag is set. Therefore sending AT's can occur only once. If a further telegram has to be send, a new MDT must be received containing the expected address of the drive.

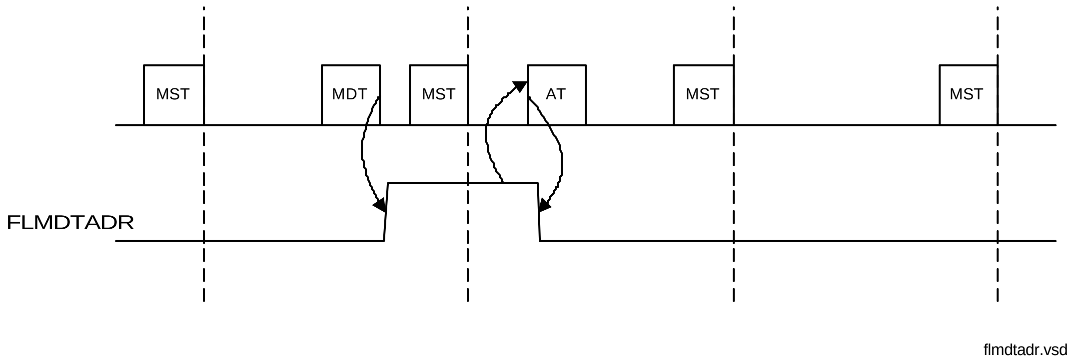

Figure 5: FLMDTADR

2.10 Bug Fix „Asynchronous Access to Dual-Port-RAM (DPR)“

Via the DPR the internal telegram processing unit and the external micro processor (µP) have access to common data structures. These data structures contain status and control information for sending and receiving telegrams.

When doing asynchronous access , the µP is reading and writing these data structures regardless of the point in time of the transmission cycle. The telegram processing unit reads data from the DPR, modifies them and writes them back to the DPR. In case the µP is writing new data to the DPR during this time, it can happen that certain control information of the tlegram processing unit are over written with wrong data.

This problem can also occur. In case the µP is doing bit manipulations (read, change, Write back) to the data stored in the DPR.

There will be no global fix for the problem with asynchronous access to the DPR. Instead for two problems, that turned out to be the most critical issues in practical use, special solutions are implemented. This is to help to avoid access conflict due to this issue.

2.10.1 Controlling the Double Buffer (VAL-Bit)

2.10.1.1 Error Description

The VAL bit controls the usage of the double buffer for the telegram data. It is located in the telegram header. In case data are to be send, the µP is programming this bit. Depending of the bit status, the SERCOS chip select the data to be send. The telegram header for the next following telegram, and so the VAL bit, are read at the end of the actual telegram. At the start time of the transmit telegram the telegram header (control word 0) is written back to the DPR in certain modes (transmit telegram, EN=1) as status information in the telegram header have changed. In case the µP has written new information for the VAL bit during the time between two telegrams, the new VAL bit information is overwritten with its old value by the telegram processor. This problem can be seen only during transmit telegram, because when receiving telegrams, only the telegram processor can manipulate the VAL bit.

2.10.1.2 Fixing Errors

The time period when access to the telegram header is not allowed, should be limited to some clock cycles at start of the transmit telegram. To achieve this , the VAL bit is read from the telegram header at start of a transmit telegram again, all other data of the telegram header (ADR, DMA, DBUF and EN) will NOT be read again. If the telegram header must be written back to the DPR (Mode EN=1), the last read VAL bit value is written together with the telegram header. Using this sequence, the µP can program a new VAL bit between two telegrams. This new VAL bit is then used for the next transmit telegram.

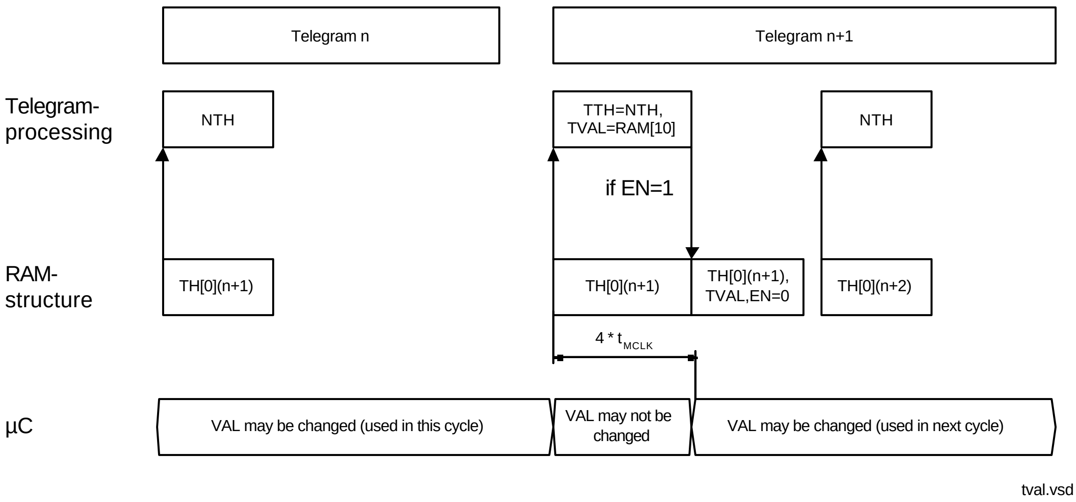

Figure 6: Read/write of VAL-Bit for transmit telegrams

REFFORMATVERBINDENFigure 6 shows this sequence. After start of a telegram the telegram header of the next expected telegram is written into register NTH of the telegram processor. When the next telegram starts NTH is copied to register TTH and the value of VAL is read again from the DPR (for transmit telegrams only). If EN = 1, then the value EN = 0 must be written to the DPR. As only complete words can be written to the DPR, all other control bits in the telegram header are written as well. The value of VAL, previously read, is now replaced by the content of TVAL. While reading the telegram header and write back, the µP may not write the telegram header information.

In order to ensure that the VAL bit for controlling the double buffer will be read only at a valid point in time, following sequence may apply:

1. the µP determines the actual point in time of the SERCOS cycle
2. the µP checks if there is enough time left to start the transmit telegram (TCNTLT < tstart - dT). The difference in time dT depends on speed of the bus interface and frequency of MCLK
3. If there is enough time, VAL can be programmed (VAL becomes valid even in the actual cycle)
4. If there is not enough time, the system has to wait until the time left is longer than tstart + 4 (VAL becomes valid in the next following cycle)

NOTE:
The sequence as described above is already implemented in the SERCON410B. For the new SERCON816, this sequence is to be checked and corrected in case it is possible. The user has to be aware of the fact that the problem of the double buffer access is caused by different issue, which is not contained in the volume of this development contract!

2.10.2 Control word for Service-Container

2.10.2.1 Error Description

Some application show problems when writing the control word for the Service-Container. In this application the control word is written again at the end of a receive telegram by the µP. To do so, the µP continuosly requests the status bit of the interrupt of the end of the receive telegram (INT_REND). If the status bits indicate the end of the telegram, the control word of the service container is written again by the µP. Now conflicts of access happen between µP and telegram processor, as the telegram processor also starts writing to the service container at the end of a receive telegram.

2.10.2.2 Solution

A new interrupt is defined (INT_RSCEND), indicating the end of the working phase of the telegram processor to the service container. This new interrupt INT_RSCEND becomes active, at the end of a receive telegram, if there are no service container that need to be worked on or in case the work is completed. The status and control bits of this new interrupt are implemented in the watch dog control register (28H).

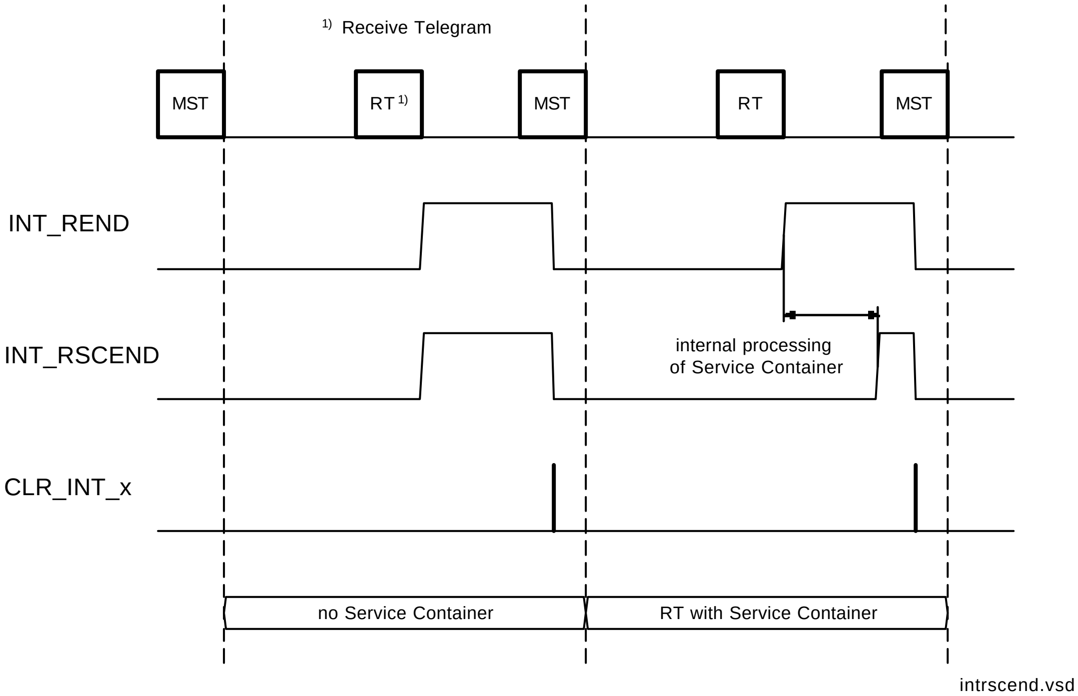

Figure 7: Interrupt RSCEND

2.11 Control Register

2.11.1 Changed Control Registers

2.11.1.1 Register VERSION (00H)

In Address 0 of the control register, the actual version of the various revisions of the SERCON chip can be read.

ASIC	VERSION (Addr. 0H)
SERCON410B	0002H
SERCON816	0010H

2.11.1.2 Register MCLKDIV, MCLKST (0EH)

The divider for time base MCLKDIV and its start value is extended by one bit, to be able to divide the higher clock frequency of the SERCON816.

ASIC	MCLKDIV	MCLKST
SERCON410B	0EH.4-0	0EH.12-8
SERCON816	0EH.5-0	0EH.13-8

2.11.1.3 Register NDIVCLK (20H)

Addr	Bit	Name	R/W	Value	Function
20H	7-0	NDIVCLK	R/W		Number of DIV_CLK cycles for one SERCOS cycle (DIVCLKMODE = 0) or number of SERCOS cycles after which a DIV_CLK pulse is generated (DIVCLKMODE = 1)
	8	POLDIVCLK	R/W	0 1	DIV_CLK Pulse 1-aktive DIV_CLK Pulse 0-aktive
	9	DIVCLKMODE	R/W	0 1	As for SERCON410B (reset): DIV_CLK becomes active N times in each SERCOS cycle New mode DIV_CLK becomes active once after N SERCOS cycles
	15-10		R	0	NOT USED

2.11.2 SERCON816 NEW Control Registers

Addr	Bit	Name	R/W	Value	Function
28H	0	WDOG_START	W	0 1	No Action Watchdog switch ON
		WDOG_STAT	R	0 1	Watchdog OFF (Reset) Watchdog ON
	1	INT_WDOG	R	0 1	Watchdog NOT Active Watchdog Active
		CLR_INT_WDOG	W	0 1	No Action Clear INT_WDOG
	2	WDOUT_SET	W	0 1	No Action Set Enable Output WDOGN
		WDOUT_STAT	R	0 1	Disable Output WDOGN (Reset) Enable Output WDOGN
	3	EN0_INT_WDOG	R/W	0 1	INT_WDOG does not trigger INT0 INT_WDOG triggers INT0
	4	EN1_INT_WDOG	R/W		Enable INT1
	5	WDOG_MSTEN	R/W	0 1	Trigger via internal MST Start locked Master: Trigger via MST enabled Slave: No Function
	6	INT_RSCEND	R	0 1	Interrupt RSCEND (End Service-Container processing after receive telegram) not activated Interrupt RSCEND became active
		CLR_RSCEND	W	0 1	No Action Clear INT_RSCEND
	7	EN0_INT_RSCEND	R/W	0 1	INT_RSCEND does not trigger INT0 INT_RSCEND triggers INT0
	8	EN1_INT_RSCEND	R/W	0 1	INT_RSCEND does not trigger INT1 INT_RSCEND triggers INT1
29H	7-0	WDOG_TRIG	W	42H	Software trigger for Watchdog
2AH	15-0	TWDOG	R/W		Watchdog time constant